AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (Canceled).

Claim 2 (Currently Amended): The process as claimed in claim [[1]] 22, wherein said etchant further contains at least one of water and hydrogen peroxide solution.

Claim 3 (Currently Amended): The process as claimed in claim [[1]] 22, wherein said etchant has a composition tailored such that, in said step c), an etching rate of said stepped structure and an etching rate of said second III-V compound semiconductor layer of said composite structure, are substantially equal.

Claim 4 (Original): The process as claimed in claim 3, wherein said step a) is performed such that said second III-V compound semiconductor layer has a thickness that is substantially equal to a product of an etching rate of the InP layer using said etchant and an etching time of said step c).

Claim 5 (Currently Amended): The process as claimed in claim [[1]] 22, wherein said etchant has a composition tailored such that, in said step c), an etching rate of said stepped structure

is lower than an etching rate of said second III-V compound semiconductor layer of said composite structure.

Claim 6 (Canceled).

Claim 7 (Currently Amended): The process as claimed in claim [[6]] 24, wherein said ~~further~~ second etchant further contains at least one of water and hydrogen peroxide solution.

Claim 8 (Original): The process as claimed in claim 7, wherein the relationship between an etching time T_1 in said step c) and an etching time T_2 in said step d) is determined in accordance with an equation:

$$(V_2 - V_1) \times T_1 = (V_3 - V_4) \times T_2,$$

where V_1 is an etching rate of the InP layer in said step c);

V_2 is an etching rate of said second III-V compound semiconductor layer in said step c);

V_3 is an etching rate of the InP layer in said step d); and

V_4 is an etching rate of said second III-V compound semiconductor layer in said step d).

Claim 9 (Currently Amended): The process as claimed in claim [[1]] 22, wherein said etchant has a composition tailored such that, in said step c), an etching rate of said stepped structure

is greater than an etching rate of said second III-V compound semiconductor layer of said composite structure.

Claim 10 (Currently Amended): The process as claimed in claim 9, wherein said ~~further~~ etchant further contains at least one of water and hydrogen peroxide solution.

Claim 11 (Canceled).

Claim 12 (Currently Amended): The process as claimed in claim [[11]] 25, wherein the relationship between an etching time T_1 in said step c) and an etching time T_2 in said step d) is determined in accordance with an equation:

$$(V_1 - V_2) \times T_1 = (V_4 - V_3) \times T_2,$$

where V_1 is an etching rate of the InP layer in said step c);

V_2 is an etching rate of said second III-V compound semiconductor layer in said step c);

V_3 is an etching rate of the InP layer in said step d); and

V_4 is an etching rate of said second III-V compound semiconductor layer in said step d).

Claims 13-14 (Canceled).

Claim 15 (Currently Amended): The process as claimed in claim [[14]] 26, wherein said ~~further~~ second etchant further contains at least one of water and hydrogen peroxide solution.

Claim 16 (Original): The process as claimed in claim 15, wherein the relationship between an etching time T_1 in said step c) and an etching time T_2 in said step e) is determined in accordance with an equation:

$$V_1 \times T_1 = (V_4 - V_3) \times T_2,$$

where V_1 is an etching rate of the InP layer in said step c);

V_3 is an etching rate of the InP layer in said step e); and

V_4 is an etching rate of said second III-V compound semiconductor layer in said step e).

Claim 17 (Currently Amended): The process as claimed in claim [[1]] 22, wherein, after said step c), said stepped structure of said etched structure, is provided with a planarized surface formed of a (100), (011) or (0-1-1) surface.

Claim 18 (Original): The process as claimed in claim 17, wherein said planarized surface is substantially flush with the surface of said first III-V compound semiconductor layer.

Claim 19 (Currently Amended): The process as claimed in claim [[1]] 22, wherein, after said step c), said stepped structure of said etched structure, is provided with a planarized surface near a (100), (011) or (0-1-1) surface.

Claim 20 (Currently Amended): The process as claimed in claim [[1]] 22, wherein said second III-V compound semiconductor layer has a composition ~~chosen~~ selected from [[a]] the group consisting of InP, InGaAs, InAs, InGaP, InGaAsP and GaInNAs.

Claim 21 (Currently Amended): The process as claimed in claim [[1]] 22, wherein said first III-V compound semiconductor layer has a composition ~~chosen~~ selected from [[a]] the group consisting of InGaAs and InGaAsP.

Claim 22 (New): A process of manufacturing a semiconductor device, comprising the steps of:

a) forming a stacked structure of a first III-V compound semiconductor layer containing In and having a composition different from InP and a second III-V compound semiconductor layer containing In, said second III-V compound semiconductor layer being formed directly on said first III-V compound semiconductor layer, where said second III-V compound semiconductor layer is disposed above said first III-V compound semiconductor layer;

b) growing an InP layer at regions adjacent said stacked structure to form a stepped structure of InP, said stepped structure and said stacked structure together defining a composite structure; and

c) wet-etching said composite structure using an etchant containing hydrochloric acid and acetic acid, to produce an etched structure.

Claim 23 (New): The process of claim 22, said step of forming, further comprising:

forming a pattern covering said second III-V compound semiconductor layer on said stacked structure, wherein said second III-V compound semiconductor layer is protected by said pattern upon wet-etching said composite structure.

Claim 24 (New): The process as claimed in claim 5, further comprising the step of:

d) second wet-etching said etched structure using a second etchant containing hydrochloric acid and acetic acid to produce a planarized structure, said second etchant having a composition tailored such that an etching rate of said stepped structure is greater than an etching rate of said second III-V compound semiconductor layer, of said etched structure.

Claim 25 (New): The process as claimed in claim 9, further comprising the step of:

d) second wet-etching said etched structure using a second etchant containing hydrochloric acid and acetic acid to obtain a planarized structure, said second etchant having a composition

tailored such that an etching rate of said stepped structure is smaller than an etching rate of said second III-V compound semiconductor layer, of said etched structure.

Claim 26 (New): The process as claimed in claim 23, further comprising the step of:

d) removing said pattern after said wet-etching; and

e) second wet-etching said etched composite using a second etchant containing hydrochloric acid and acetic acid to produce a planarized structure, said second etchant having a composition tailored such that an etching rate of said stepped structure is smaller than an etching rate of said second III-V compound semiconductor layer, of said etched structure.